IN THE CLAIMS:

Please amend claims 1, 2, 4-7, 9-12, 14-17, 19 and 20, and add new claims 21-24 as follows:

1. (Currently amended) An electric characteristic evaluating apparatus for extracting electric characteristics of a semiconductor device by numerically solving physical equations describing physical phenomenon in a semiconductor device comprising:

an integral value calculator configured to integrate a carrier generation and extinction speed obtained in each carrier generation and extinction mechanism by numerically solving the physical equations, in the each carrier generation and extinction mechanism within a semiconductor region, and issue the result obtained by integration respectively.

2. (Currently amended) The electric characteristic evaluating apparatus according to claim 1, wherein the volume integration is effected [[on]] by the carrier generation and extinction mechanism having the dimension of length^{-3} time^{-1}, the surface integration is effected [[on]] by the carrier generation and extinction mechanism having the dimension of length^{-2} time^{-1}, and the line integration is effected [[on]] by the carrier generation and extinction mechanism having the dimension of length^{-1} time^{-1}.

3. (Original) The electric characteristic evaluating apparatus according to claim 1, wherein the carrier generation and extinction mechanism includes a SRH process, impact ionization, and inter-band tunneling.

4. (Currently amended) The electric characteristic evaluating apparatus according to claim 1, wherein said integral value calculator issues an output by multiplying a

~~charge amount~~ prime charge to each integral value of the each carrier generation and extinction mechanism.

5. (Currently amended) The electric characteristic evaluating apparatus according to claim 1, wherein the electric characteristics are extracted repeatedly by varying a bias condition to the semiconductor device.

6. (Currently amended) An electric characteristic evaluating method for extracting electric characteristics of a semiconductor device by numerically solving physical equations describing physical phenomenon in a semiconductor device comprising ~~the step of~~ :

integrating a carrier generation and extinction speed obtained in each carrier generation and extinction mechanism by numerically solving the physical equations, in the each carrier generation and extinction mechanism within a semiconductor region; and

issuing the result obtained by integration respectively.

7. (Currently amended) The electric characteristic evaluating method according to claim 6, wherein the volume integration is effected [[on]] by the carrier generation and extinction mechanism having the dimension of length^{-3} time^{-1}, the surface integration is effected [[on]] by the carrier generation and extinction mechanism having the dimension of length^{-2} time^{-1}, and the line integration is effected [[on]] by the carrier generation and extinction mechanism having the dimension of length^{-1} time^{-1}.

8. (Original) The electric characteristic evaluating method according to claim 6, wherein the carrier generation and extinction mechanism includes a SRH process, impact ionization, and inter-band tunneling.

9. (Currently amended) The electric characteristic evaluating method according to claim 6, wherein an output is issued by multiplying a ~~charge amount~~ prime charge to each integral value of the each carrier generation and extinction mechanism.

10. (Currently amended) The electric characteristic evaluating method according to claim 6, wherein the electric characteristics are extracted repeatedly by varying a bias condition to the semiconductor device.

11. (Currently amended) An electric characteristic evaluating program for extracting electric characteristics of a semiconductor device by numerically solving physical equations describing physical phenomenon in a semiconductor device, comprising ~~and making a computer system execute the process of~~:

instructions configured to integrate ~~an integral value calculating process of integrating~~ a carrier generation and extinction speed obtained in each carrier generation and extinction mechanism by numerically solving the physical equations, in the each carrier generation and extinction mechanism within a semiconductor region, and ~~issuing~~ issue the result obtained by integration respectively.

12. (Currently amended) The electric characteristic evaluating program according to claim 11, wherein the volume integration is effected [[on]] by the carrier generation and extinction mechanism having the dimension of length^{-3} time^{-1}, the surface integration is effected [[on]] by the carrier generation and extinction mechanism having the dimension of length^{-2} time^{-1}, and the line integration is effected [[on]] by the carrier generation and extinction mechanism having the dimension of length^{-1} time^{-1}.

13. (Original) The electric characteristic evaluating program according to claim 11, wherein the carrier generation and extinction mechanism includes a SRH process,

impact ionization, and inter-band tunneling.

14. (Currently amended) The electric characteristic evaluating program according to claim 11, wherein an output is issued by multiplying a ~~charge amount~~ prime charge to each integral value of the each carrier generation and extinction mechanism.

15. (Currently amended) The electric characteristic evaluating program according to claim 11, wherein the electric characteristics are extracted repeatedly by varying a bias condition to the semiconductor device.

16. (Currently amended) A semiconductor device manufacturing method for extracting electric characteristics of a semiconductor device by numerically solving physical equations describing physical phenomenon in a semiconductor device, determining the manufacturing condition of semiconductor device from the extracted electric characteristics, and manufacturing the semiconductor device on the basis of the determined manufacturing condition comprising ~~the step of~~:

integrating a carrier generation and extinction speed obtained in each carrier generation and extinction mechanism by numerically solving the physical equations, in the each carrier generation and extinction mechanism within a semiconductor region, and issuing the result obtained by integration respectively; and

determining the manufacturing condition of the semiconductor device having the desired electric characteristics on the basis of the result obtained by integration.

17. (Currently amended) The semiconductor device manufacturing method according to claim 16, wherein the volume integration is effected [[on]] by the carrier generation and extinction mechanism having the dimension of length^{-3} time^{-1}, the surface integration is effected [[on]] by the carrier generation and extinction mechanism

having the dimension of length^{-2} time^{-1}, and the line integration is effected [[on]] by the carrier generation and extinction mechanism having the dimension of length^{-1} time^{-1}.

18. (Original) The semiconductor device manufacturing method according to claim 16, wherein the carrier generation and extinction mechanism includes a SRH process, impact ionization, and inter-band tunneling.

19. (Currently amended) The semiconductor device manufacturing method according to claim 16, wherein an output is issued by multiplying a ~~charge amount~~ prime charge to each integral value of the each carrier generation and extinction mechanism.

20. (Currently amended) The semiconductor device manufacturing method according to claim 16, wherein the electric characteristics are extracted repeatedly by varying a bias condition to the semiconductor device.

21. (New) The electric characteristic evaluating apparatus according to claim 1, further comprising an analyzer configured to extract the plurality of the generation and extinction speeds by numerically solving the physical equations.

22. (New) The electric characteristic evaluating method according to claim 6, further comprising extracting the plurality of the generation and extinction speeds by numerically solving the physical equations.

23. (New) The electric characteristic evaluating program according to claim 11, further comprising instructions configured to extract the plurality of the generation and extinction speeds by numerically solving the physical equations.

24. (New) The semiconductor device manufacturing method according to claim 16, further comprising extracting the plurality of the generation and extinction speeds by

numerically solving the physical equations.